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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/384,504	08/27/1999	JOHN W. MARSHALL	112025-0166	7925

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EXAMINER	
BRODA, SAMUEL	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/384,504	MARSHALL ET AL.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicants' Amendment received on 12 February 2003 as part of a Continued Prosecution Application. Claims 13-17 were added; claims 1-17 are pending.

Claim Rejections - 35 U.S.C. § 112, First Paragraph

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2.1 Claims 1-17 are rejected under 35 U.S.C. 112, first paragraph.

2.2 Regarding claims 1-4, 9-13, and 16, these claims are rejected under 35 U.S.C. 112, first paragraph, because the Specification does not reasonably provide enablement for generating an approximate mathematical model of a remaining or second portion of a system. The Specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

2.3 Regarding claims 5-8, 14-15, and 17, these claims are rejected under 35 U.S.C. 112, first paragraph, because the Specification, does not reasonably provide enablement for estimating operation of system using hierarchical analysis mathematical functions. The

Specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

2.4 In response to the rejection of the claims under Section 102(b) made in Paper No. 6, Applicants amended each independent claim to denote the generation of an approximate "mathematical" model based upon hierarchical analysis. In the remarks on pages 3-7 of the Amendment, Applicants argue that the McDonald et al reference fails to disclose such mathematical models.

However, Applicants failed to indicate the support in the Specification for the "mathematical" models as appearing in the amended claims. The portion of the Specification that most closely supports Applicants' amendment to the claims appears to be at page 12 lines 1-15, which states in part:

> As shown schematically in Figure 4, in the HA model 150 of design 100, functions 82, 84, and 86 are used. In essence functions 82, 84, 86 are mathematical functional abstractions, based upon the physical characteristics of the proposed design in the databases 46, 48 . . . More specifically, function 82 essentially is an approximate mathematical model of the overall timing operation of the module 65 . . . Similarly, function 84 essentially is an approximate mathematical model of the overall timing operation of the connection 70 . . . Also similarly, function 86 essentially is an approximate mathematical model of the overall timing operation of the module 67 . . .

(Emphasis supplied.)

While this description of functions 82, 84, 86 each comprise an "approximate mathematical model" suggests the purpose of each function is to approximate timing operations,

the Specification fails to provide any further description of a kind or type of mathematical model. When compared to the amended claims, it appears that the scope of the claims cover any mathematical model.

2.5 Regarding claims 1-17, these claims are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

A review of the Specification and drawings indicates that pages 13-17 of the Specification describe the dividing of a system into a portion modeled by physical characteristics and a portion modeled using hierarchical analysis.

While the Specification at page 16 lines 5-11 appears to discuss one empirically-determined rule for selecting a portion of a circuit for simulation using physical characteristics, no flowcharts or text description in the Specification appears to describe how to program Applicants' claimed invention. Similarly, no flowcharts or text in the Specification appear to describe how to interconnect the computer components. These components include a user interface and hardware for inputing and processing netlists and SPEF or SDF data. Instead, the Specification appears to describe the general features of Applicants' claimed invention as applied to the schematic circuit models appearing in the drawings.

In this situation, the MPEP Section 2106.02 appears applicable. This section states in-part at page 2100-27 column 1 paragraph 2 (Feb. 2003):

> While no specific universally applicable rule exists for recognizing an insufficiently disclosed application involving computer programs, an examining guideline to generally follow is to challenge the sufficiency of such disclosures which fail to include either the computer program itself or a reasonably detailed flowchart which delineates the sequence of operations the program must perform.

Taken as a whole, only with undue experimentation could one reasonably skilled in the art make and/or use the invention described in the specification.

Applicants are encouraged to review MPEP Section 2106.02 regarding approaches to traversing this rejection.

Claim Rejections - 35 U.S.C. § 112, Second Paragraph

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3.1 Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

3.2 The term "approximate mathematical model" in claims 1, 9, 13, 15, and 16-17 is a relative term which renders the claim indefinite. The term "approximate mathematical model" is not defined by either claim, the specification does not provide a standard for ascertaining the

requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The term "hierarchical analysis mathematical functions" in claims 5 and 14 is a relative term which renders the claim indefinite. The term "hierarchical analysis mathematical functions" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

In response to the rejection of the claims under Section 102(b) made in Paper No. 6, Applicants amended each independent claim to denote the generation of an approximate "mathematical" model based upon hierarchical analysis. In the remarks on pages 3-7 of the Amendment, Applicants argue that the McDonald et al reference fails to disclose such mathematical models.

However, Applicants failed to indicate the support in the Specification for the "mathematical" models as appearing in the amended claims. The portion of the Specification that most closely supports Applicants' amendment to the claims appears to be at page 12 lines 1-15, which states in part:

> As shown schematically in Figure 4, in the HA model 150 of design 100, functions 82, 84, and 86 are used. In essence functions 82, 84, 86 are mathematical functional abstractions, based upon the physical characteristics of the proposed design in the databases 46, 48 . . . More specifically, function 82 essential is an approximate mathematical model of the overall timing operation of the module 65 . . . Similarly,

function 84 essentially is an approximate mathematical model of the overall timing operation of the connection 70 . . . Also similarly, function 86 essentially is an approximate mathematical model of the overall timing operation of the module 67 . . . (Emphasis supplied.)

While this description of functions 82, 84, 86 each comprise an "approximate mathematical model" suggests the purpose of each function is to approximate timing operations, the Specification fails to provide any further description of a kind or type of mathematical model and also fails to provide a standard for ascertaining the requisite degree.

3.3 Taken as whole, one of ordinary skill in the art would not be reasonably apprised of the scope of the invention because of the uncertainty regarding what constitutes an "approximate mathematical model" and "hierarchical analysis mathematical functions."

3.4 For the purpose of further claim examination, the Examiner will presume that an "approximate mathematical model" or "hierarchical analysis mathematical functions" correspond to an equation in mathematical form that is capable of being programmed in a computer.

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> . . .
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.1 Claims 1-12 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shepard et al, "Design Methodology for the S/390 Parallel Enterprise Server G4 Microprocessors", IBM Journal of Research and Development, Vol. 41 No. 4/5, pp. 515-547 (July 1997) (prior art cited in Paper No. 6 and supplied to Applicants).

4.2 Regarding claim 1, Shepard et al teaches a computerized method for use in simulating an operation of an electronic system, the method being carried out using a computer system, the method comprising:

generating a physically-accurate description of a first portion of the system, the physically-accurate description comprising actual physical characteristics of the first portion [physically-accurate description of G4 microprocessor at "global" level including global wires and global timing assertions; see page 516 column 2 through page 517column 1];

generating an approximate mathematical model of a remaining portion of the system, the model being based upon hierarchical analysis of the remaining portion [static timing analysis using hierarchical approach using "Pathmill" tool at macro level used to abstract timing into "black" or "gray" boxes (pages 528-530), with results fed to IBM "EinsTimer" to generate an approximate mathematical models of current (page 530) and voltage (page 531)]; and

using both the physically-accurate description and the approximate model to simulate the operation of the system [models used as part of design methodology, metrics for design quality and design abstraction; see page 516-517].

Therefore, Shepard et al anticipates claim 1.

4.3 Regarding independent claims 5, 9, and 16, claims 5 and 16 are system claims corresponding to claim 1, and claim 9 is the computer program product claim corresponding to claim 1. Claims 5 and 9 are anticipated using the analysis of claim 1, where the "hierarchical analysis mathematical function" of claim 5 corresponds to either the current function on page 530 or the voltage function on page 531.

4.4 Regarding claims 2-3, 6-7, and 10-11, the Pathmill macro-level timing analysis includes a configuration file contains "hints" corresponding to simulation optimization rules for how to handle difficult circuit topologies and thus reduce simulation error. See page 528 column 1 paragraph 3.

4.5 Regarding claims 4, 8 and 11, Shepard et al teaches use of the Pathmill and EinsTimer simulators to handle timing operations.

Claim Rejections - 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.1 Claims 13-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shepard et al, in view of Luk et al, "Visualising Reconfigurable Libraries for FPGAs",

IEEE Conference Record of the Thirty-First Asilomar Conference on Signals, Systems & Computers, Vol. 1, pp. 389-393 (November 1997).

5.2 Regarding independent claim 13, this method claim differs from independent claim 1 by including a step where the electronic system to be simulated is divided into two portions while represented on a user interface. Shepard et al does not appear to teach use of a user interface as part of the macro timing abstractions conducted in Pathmill in conjunction with the Verity equivalence checking.

Luk et al teaches the desirability of circuit simulation using a visualization system including a user interface that provides views of design structure and behavior. See page 390 column 1. The simulated circuit designs include reconfigurable FPGAs that with individual components reconfigurable using virtual control elements. See page 392 column 1. According to Luk et al, such as system should:

> . . . benefit both library users and suppliers, since they can be used (a) to show the internal structure of a design, (b) to illustrate effective usage of library components, and (c) to present the consequences of parametrising designs in different ways.

5.3 Regarding claim 13, it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to have incorporated the user interface features of Luk et al into the design methodology of Shepard et al, because such a combination would permit the user to better visualize the consequences of parameterizing designs using the design abstraction of Shepard et al.

5.4 Regarding claims 14-15 and 17, these claims correspond to the system and computer program product claims of claim 13, and are rejected using the analysis of claim 13 above.

Applicants' Arguments

6.1 Applicants first argue in the Amendment at pages 6-9 that the rejections made under Section 112 are inapplicable to the claims because the Specification identifies "approximate mathematical" models at several locations and that the Specification also states that the "hierarchical analysis" technique is known in the art, with Applicants arguing that "a person of ordinary skill in the art of designing computer chips and doing analysis on the chips will be familiar with the HA method." (Amendment, page 8 paragraph 2.)

6.2 Applicants then argue in the Amendment at pages 11-12 that the rejection made under Section 102 using the reference Shepard et al is inapplicable to the claims because "Shepard simply uses two levels of approximation, first his approximate black or gray boxes, and then he combines them using his pi-model for interconnection of his boxes." (Amendment, page 12 paragraph 2.)

Examiner's Reply

7. In response to Applicants' arguments, the Examiner respectfully disagrees for the following reasons:

7.1 Regarding the rejections made under Section 112, the Specification and drawings do not appear to describe how to make the claimed invention, and the arguments made regarding the level of knowledge by one of ordinary skill in the art are not supported with any facts or documentary evidence.

7.2 Regarding the rejection made under Section 102, the pointers to the reference have been modified to better illustrate the correspondence between Applicants' claims and the reference's use of hierarchical analysis to design a microprocessor using global and macro abstractions.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure. Reference to Li et al, "Optimization of Analog Modeling and Simulation", IEEE 5th International Conference on Solid-State and Integrated Circuit Technology, pp.385-388 (October 1998), is cited as teaching the partitioning of circuits in portions modeled at a transistor level using SPICE with the remaining circuit portions modeled using analog HDL.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

(703) 746-7238 --- for communications after a Final Rejection has been made;

(703) 746-7239 --- for other official communications; and

(703) 746-7240 --- for non-official or draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER